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<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b> ( Not for submission under 37 CFR 1.99)	Application Number		10750714
	Filing Date		2003-12-31
	First Named Inventor	Gonzalez	
	Art Unit	2181	
	Examiner Name	Benjamin P. Geib	
	Attorney Docket Number	PA2683US	

U.S.PATENTS						
Examiner Initial*	Cite No	Patent Number	Kind Code <sup>1</sup>	Issue Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear
	1	6467009		2002-10-15	Winegarden	
	2	6505241		2003-01-07	Pitts	
	3	6557092		2003-04-29	Callen	
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9	6744274		2004-06-01	Arnold	
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**U.S. PATENT APPLICATION PUBLICATIONS**

Examiner Initial*	Cite No	Publication Number	Kind Code <sup>1</sup>	Publication Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear
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**FOREIGN PATENT DOCUMENTS**

Examiner Initial*	Cite No	Foreign Document Number <sup>3</sup>	Country Code <sup>2</sup>	Kind Code <sup>4</sup>	Publication Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear	T <sup>5</sup>
	1	0 507 507	EP		1992-07-10	American Telephone		<input type="checkbox"/>
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4	152355	TW		2002-07-10	Adaptive Silicon, Inc.	<input type="checkbox"/>
5	152994	TW		2002-07-22	Adaptive Silicon, Inc.	<input type="checkbox"/>
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Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>5</sup>
	1	RUPP et al.; U.S. Patent Application No. 10/746,018, entitled "Architecture and Method for Reconfigurable Data Path Processing," filed Dec. 23, 2003.	<input type="checkbox"/>
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7	GONZALEZ, RICARDO E., "Xtensa: A Configurable and Extensible Processor," March-April 2000, IEEE Micro, pp 60-70.	<input type="checkbox"/>
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9	HWANG, KAI, "Advanced Computer Architecture: Parallelism, Scalability, Programmability," 1993, McGraw Hill, pp. 182-183.	<input type="checkbox"/>
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11	JACOB et al, "Memory Interfacing and Instruction Specification for Reconfigurable Processors," 1999; ACM.	<input type="checkbox"/>
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14	TANENBAUM, ANDREW S., "Modern Operating Systems," 2001, 2nd edition, Prentice Hall, New Jersey, p. 31.	<input type="checkbox"/>
15	TAYLOR, MICHAEL BEDFORD, et al., "The Raw Microprocessor: A Computational Fabric for Software Circuits and General-Purpose Programs," Microarchitecture, IEEE Micro, March-April 2002, pp 25-35.	<input type="checkbox"/>
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17	YE, Z.A. et al., "CHIMAERA: A high-performance architecture with a tightly-coupled reconfigurable functional unit," June 10-14, 2000, Proc. of the 27th International Symposium on Computer Architecture, pp. 225-235.	<input type="checkbox"/>

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18	<a href="http://www.tensilica.com/products/xtensa_overview.htm">http://www.tensilica.com/products/xtensa_overview.htm</a> Xtensa Processor Overview	<input type="checkbox"/>
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